IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Divakaruni et al.		**Conf. No.**:	1387
Serial No.:	10/707,388	**Art Unit**:	2891
Filed:	12/10/2003	**Examiner**:	Fulk, Steven J.
Title:	SILICIDE RESISTOR IN BEOL LAYER OF SEMICONDUCTOR DEVICE AND METHOD	**Docket No.:**	FIS920030274 (IBMF-0032)

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Commissioner for Patents
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicants respectfully request a panel of experienced Examiners perform a detailed review of appealable issue for the above-identified patent application pursuant to the Pre-Appeal Brief Conference Pilot Program. Notice of Appeal has been filed together with this Request.

Applicants submit that the above-identified application is not in condition for appeal because the final rejection is clearly defective due to errors in facts and in law as the relied upon references clearly miss some claim features. Claims 12-18 and 20 are pending in this application.

In the Office Action, claims 12-20 are rejected under 35 USC §112, second paragraph, as allegedly being indefinite. Specifically, the Office interprets "probable" in the definition of "damaging temperature" as "establishing a probability" and asserts that "the specification does not establish a probability of damage at the silicidation temperature[.]" (Office Action at page 2). Applicants respectfully disagree because the Office applies an apparently non-applicable interpretation of the term "probable". The Office is improperly importing this limitation into the claims. This is not permissible. *Altiris Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003). The claim language states "wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers". This language on its face is clear to the skilled artisan as silicidation temperature, damaging temperature and BEOL layers are all clear to a person of ordinary skill in the art. This is not clear to the Examiner who states that; "Because the specification does not establish a probability of damage at the silicidation temperature, it is not sufficiently clear whether or not damage occurs to the BEOL layers." Applicant has provided an invention that allows a passive resistor to be processed without high temperature anneals that would damage other BEOL wiring structures [paragraph 0004]. The BEOL layers can be of various materials [paragraph 0021] and the silicidation temperature is dependent on the silicide [paragraph 0020]. Thus, a damaging temperature to the BEOL layers depends on certain factors that are known to the skilled artisan. Either the BEOL wiring layers are damaged when processed or they or not, and this determination can be made without undue experimentation through a test of the BEOL layers after processing. In view of the foregoing, Applicants respectfully request withdrawal of the rejection under 35 USC §112, second paragraph.

Claims 12, 18 and 20 are rejected under 35 U.S.C. §103(a) as allegedly being anticipated by Yoo et al. (US 6,168,984), hereinafter "Yoo", and claims 13-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yoo in view Wolf, *Silicon Processing for the VLSI Era*, 1990, Volume II, pp 146, 176, 193 hereinafter "Wolf." Applicants respectfully submit that the claimed subject matter is allowable for the reasons stated below.

With respect to anticipation rejection of claims 12, 18 and 20, the Examiner asserts that Yoo discloses a silicide resistor formed of a poly-silicon layer and a tungsten silicide layer. The Examiner asserts that the structure referenced in Figure 13 of Yoo has an inherent resistance and thus considered a resistor in one of a plurality of BEOL layers (formed from an interlayer dielectric over FEOL layers 1-17, layer 31 is a second BEOL layer, thus 27 and 31 are a plurality), the silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. This argument ignores the teaching of Yoo. The structure referred to in Yoo is a bitline structure (col. 8 lines 65-66) in an opening (col. 8, lines 48-51). Thus, the characterization that Yoo teaches a silicide resistor in a trough is faulty. A bitline is not a resistor and a bitline structure positioned in an opening that connects each side of insulating layer 27 is not a resistor positioned in a trough. Therefore, Yoo does not show every element of the instant invention and the anticipation rejection is defective.

With respect to claims 13-17 Wolf is cited for teaching group VII silicides. Such disclosures of the silicides substituted into the structure of Yoo would not produce Applicants invention. There would not be a silicide resistor as claimed but a bitline for use in a DRAM semiconductor device. In addition, both Wolf references only disclose using the silicide materials for interconnect applications, not for a resistor application as claimed in the current invention. The combination proposed could not produce a silicide resistor in a trough.

Therefore a combination of the references does not provide a *prima facia* obviousness-type rejection.

The dependent claims are believed allowable for the same reasons stated above, as well as for their own additional features.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

/Carl F. Ruoff/

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